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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/072,171

Applicant(s)

HIROKI, MASAOKI

Examiner

KEVIN M. NGUYEN

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 April 2008.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2-11 and 13-28 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 2-11 and 13-28 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date 04/04/2008
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

Application and Claims Status

Applicant's amendment and response filed on 04/04/2008 are acknowledged and entered.

In view of the amendment, the objection of claim 11 and the rejection of claim 10 stand withdrawn.

Claims 2-11 and 13-20 were pending. Applicants have added claims 25-28, amended claims 2, 3 10 and 11 . Therefore, claims 2-11, 13-20 and 25-28 are currently pending and are under consideration in this Office Action.

Response to Arguments

Applicant's arguments, see pages 12-16, filed on 04/04/2008, with respect to previous rejection have been fully considered and are persuasive. The rejection of claims 1-10 has been withdrawn.

Status of Claim(s) Objection(s) and/or Rejection(s)

All previous objection(s)/rejection(s) have been withdrawn in view of applicant's amendments of claims 2-11, 13-20 and 25-28.

New Rejection(s) - Necessitated by Amendment

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 2-5, 10, 11, 13, 14 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al (US 6,333,515, Yamaguchi) in view of Applicant admitted prior art (AAPA), and further in view of Yoshida et al. (US 7,133,015, Yoshida.)
3. **As to claim 2**, Yamaguchi teaches a method of driving a liquid crystal display device comprising:

supplying picture signals from a digital video data dividing circuit to a D/A converter circuit (the alternative embodiment of fig. 1B shows 8-bit digital video data supplying to a D/A inherits in the data driver 8);

supplying a first voltage for a first gradation from the D/A converter circuit to a pixel by first scanning signals of a gate driver in a first subframe period (the alternative embodiment of figs 34 and 35 show supplying a voltage 2.1V for a grayscale level 1 in a first field VF1 of the positive frame. The alternative embodiment of Fig. 1B, shows a scan driver 7);

supplying signals a voltage for a 0th gradation from the D/A converter circuit to the pixel by second scanning signals of the gate driver in a second subframe period (the alternative embodiment of fig. 34 shows supplying a voltage 2V for a grayscale level 0 in a second field VF2 of the positive frame, col. 12, lines 32-58);

supplying a second voltage for a second gradation from the D/A converter circuit to a pixel by third scanning signals of a gate driver in a third subframe period (the alternative embodiment of figs. 34 and 35 show supplying a voltage -2.2V for a grayscale level 2 in a third field of the negative frame, col. 12, lines 32-58);

supplying a third voltage for a third gradation from the D/A converter circuit to a pixel by fourth scanning signals of a gate driver in a fourth subframe period (the alternative

embodiment of figs. 34 and 35 show supplying a voltage -2.3V for a grayscale level 3 in a fourth field of the negative frame, col. 12, lines 32-58);

displaying first frame by displaying a first subframe and a second subframe (the alternative embodiment of fig. 7B shows the hatching area of the display for the first field and the second field, col. 12, lines 32-58);

displaying second frame by displaying a third subframe and a fourth subframe (the alternative embodiment of fig. 7B shows the hatching area as shown of the display for the third field and the fourth field, col. 12, lines 32-58),

wherein first frame period has the first subframe period and the second subframe period (the positive frame has the first field and the second field, fig. 35);

wherein second frame period has the third subframe period and the fourth subframe period (the negative frame has the third field and the fourth field, fig. 35);

wherein the first subframe period and the second subframe period are adjacent to each other (the first field and the second field are adjacent, fig. 35);

wherein the third subframe period and the fourth subframe period are adjacent to each other (the third field and the fourth field are adjacent, fig. 35);

wherein the first frame is displayed gradation acknowledged by operator's eyes; the gradation is correspond to half of the first voltage (the viewer's eyes percept the hatching area is displayed the effective voltage 3 volts by taking an average of 2 volts and 4 volts, fig. 7B)

wherein the second frame is displayed combined gradation acknowledged by operator's eye (the negative frame is displayed the effective voltage 3 volts by combining with 2 volt and 4 volts, fig. 7B),

wherein the combined gradation is correspond to the second voltage and the third voltage (the combination grayscale level of the corresponding 2 volts and 4 volts, fig. 7B).

Yamaguchi fails to teach a source driver having a D/A converter circuit. AAPA conventionally discloses a digital driver including a D/A converter circuit, page 2, lines 19-26.

It would have been obvious to a person of ordinary skill at the time the invention was made to modify Yamaguchi to have the source driver having a D/A converter circuit as conventionally disclosed by AAPA. The motivation for doing so would improve the high-speed driving of the driver in the LCD device (page 2, lines 7-13 of AAPA).

Yamaguchi and AAPA fail to teach the voltage for the 0th gradation is for displaying black-display in a screen of the liquid crystal display device.

Yoshida conventionally discloses “for the remaining three frame period, the voltage between the pixel electrode 1 and the counter electrode is 0 V. Therefore, the liquid crystal cell C shuts the light and black is displayed on the screen. (Col. 2, lines 2-5; Fig. 2).

Thus, it would have been obvious to a person of ordinary skill at the time the invention was made to modify Yamaguchi and AAPA to have the voltage for the 0th gradation is for displaying black-display in a screen of the liquid crystal display device as conventionally disclosed by Yoshida. The motivation for doing so would improve the high quality of the image being displayed, while preventing flicker and ghosts (col. 3, lines 33-36 of Yoshida.)

4. **As to claim 3**, Yamaguchi teaches a method of driving a liquid crystal display device comprising:

supplying picture signals from a digital video data dividing circuit to a D/A converter circuit (the alternative embodiment of fig. 1B shows 8-bit digital video data supplying to a D/A inherits in the data driver 8);

supplying voltages of picture signals from the D/A converter circuit to a pixel by scanning signals of a gate driver in each of plural subframe periods (the alternative embodiment of figs 34 and 35 show supplying voltages in each of plural fields. The alternative embodiment of Fig. 1B, shows a scan driver 7);

displaying one frame by displaying plural subframes (the alternative embodiment of fig. 7B shows the hatching area as shown of the display a positive frame by the plural fields),

wherein one frame period has the plural subframe periods (the positive frame has the plural field periods, fig. 7B);

wherein the plural subframe periods are adjacent to each other (the plural fields are adjacent to each other, fig. 7B);

wherein a **first voltage for a first gradation is supplied to a pixel in a first subframe period** (the alternative embodiment of figs 34 and 35 show a voltage 2.1V for a grayscale level 1 is supplied in a first field VF1 of the positive frame, col. 12, lines 32-58);

wherein **0th gradation voltage is supplied to a pixel in a second subframe period** (the alternative embodiment of figs 34 and 35 show 0th grayscale voltage level is supplied in a second field VF1 of the positive frame, col. 12, lines 32-58);

wherein a **second voltage for a second gradation is supplied to a pixel in a third subframe period** (the alternative embodiment of figs. 34 and 35 show a voltage -2.2V for a grayscale level 2 is supplied in a third field period of the negative frame, col. 12, lines 32-58);

wherein a **third voltage for a second gradation is supplied to a pixel in a fourth subframe period** (the alternative embodiment of figs. 34 and 35 show a voltage -2.3V for a grayscale level 3 is supplied in a fourth field period of the negative frame, col. 12, lines 32-58);

wherein the second voltage and the third voltage are different from each other throughout displaying the one frame (the second voltage -2.2V and the third voltage -2.3V are different).

Yamaguchi fails to teach a source driver having a D/A converter circuit. AAPA conventionally discloses a digital driver including a D/A converter circuit, page 2, lines 19-26.

It would have been obvious to a person of ordinary skill at the time the invention was made to modify Yamaguchi to have the source driver having a D/A converter circuit as conventionally disclosed by AAPA. The motivation for doing so would improve the high-speed driving of the driver in the LCD device (page 2, lines 7-13 of AAPA).

Yamaguchi and AAPA fail to teach the voltage for the 0th gradation is for displaying black-display in a screen of the liquid crystal display device.

Yoshida conventionally discloses “for the remaining three frame period, the voltage between the pixel electrode 1 and the counter electrode is 0 V. Therefore, the liquid crystal cell C shuts the light and black is displayed on the screen. (Col. 2, lines 2-5; Fig. 2).

Thus, it would have been obvious to a person of ordinary skill at the time the invention was made to modify Yamaguchi and AAPA to have the voltage for the 0th gradation is for displaying black-display in a screen of the liquid crystal display device as conventionally disclosed by Yoshida. The motivation for doing so would improve the high quality of the image being displayed, while preventing flicker and ghosts (col. 3, lines 33-36 of Yoshida.)

5. **As to claim 10**, Yamaguchi teaches a liquid crystal display device comprising:

plural pixels (a plurality of pixel "P", see Fig. 2, col. 6, lines 7-11);

a gate driving circuit (a scan driver 7, Fig. 2);

a D/A converter circuit for supplying picture signals to the pixels by scanning signals of the gate driving circuit (a D/A inherits in the data driver 8, fig. 1B);

a digital video data dividing circuit for supplying picture signals to the D/A converter circuit (fig. 1B shows video data 16 bit is dividing 8 bit for each of upper data driver 8 and lower data driver 8);

a liquid crystal whose transmittivity is changed dependently on the voltage of the picture signals supplied to the pixels (see col. 5, lines 58-61);

means for supplying voltage of picture signals from a D/A converter circuit to a pixel by scanning signals of a gate driver in each of plural subframe periods (see Figs. 7A-7D, col. 8, lines 15-27);

means for displaying one frame by displaying plural subframes (an average of 2V and 4V is (3V) is an image being displayed in one frame, see Figs. 6 and 7B, col. 8, lines 11-15, and col. 8, lines 19-24);

wherein one frame period has the plural subframe periods (the image of one frame (16.8ms) is divided into the first field (8.4ms) and second field (8.4ms) as shown in Fig. 6, col. 8, lines 13-15);

wherein the plural subframe periods are adjacent to each other (the first field and the second field are consecutive, see Fig. 7);

wherein the supplied voltages in adjacent subframe periods are different from each other throughout displaying the one frame (different voltage levels are applied to the first and second

fields, respectively, and differences in mean effective voltage occurring in individual frames. The image data of one display panel can be displayed in a half time of one frame, see col. 8, lines 28-33, and col. 7, lines 43-45); and

wherein a **first voltage for a first gradation is supplied to a pixel in a first subframe period** (the alternative embodiment of figs 34 and 35 show supplying a voltage 2.1V for a grayscale level 1 is supplied in a first field VF1 of the positive frame);

wherein **0th gradation voltage is supplied to a pixel in a second subframe period** (the alternative embodiment of figs 34 and 35 show 0th grayscale voltage level is supplied in a second field VF1 of the positive frame);

wherein a **second voltage for a second gradation is supplied to a pixel in a third subframe period** (the alternative embodiment of figs. 34 and 35 show a voltage -2.2V for a grayscale level 2 is supplied in a third field period of the negative frame);

wherein a **third voltage for a second gradation is supplied to a pixel in a fourth subframe period** (the alternative embodiment of figs. 34 and 35 show a voltage -2.3V for a grayscale level 3 is supplied in a fourth field period of the negative frame).

wherein the second voltage and the third voltage are different from each other throughout displaying the one frame (the second voltage -2.2V and the third voltage -2.3V are different).

Yamaguchi fails to teach a source driver having a D/A converter circuit. AAPA conventionally discloses a digital driver including a D/A converter circuit, page 2, lines 19-26.

It would have been obvious to a person of ordinary skill at the time the invention was made to modify Yamaguchi to have the source driver having a D/A converter circuit as

conventionally disclosed by AAPA. The motivation for doing so would improve the high-speed driving of the driver in the LCD device (page 2, lines 7-13 of AAPA).

Yamaguchi and AAPA fail to teach the voltage for the 0th gradation is for displaying black-display in a screen of the liquid crystal display device.

Yoshida conventionally discloses “for the remaining three frame period, the voltage between the pixel electrode 1 and the counter electrode is 0 V. Therefore, the liquid crystal cell C shuts the light and black is displayed on the screen. (Col. 2, lines 2-5; Fig. 2).

Thus, it would have been obvious to a person of ordinary skill at the time the invention was made to modify Yamaguchi and AAPA to have the voltage for the 0th gradation is for displaying black-display in a screen of the liquid crystal display device as conventionally disclosed by Yoshida. The motivation for doing so would improve the high quality of the image being displayed, while preventing flicker and ghosts (col. 3, lines 33-36 of Yoshida.)

6. **As to claim 11**, Yamaguchi teaches a liquid crystal display device comprising:

plural pixels (a plurality of pixel “P”, see Fig. 2, col. 6, lines 7-11);

a gate driving circuit (a scan driver 7, Fig. 2);

a D/A converter circuit for supplying picture signals to the pixels by scanning signals of the gate driving circuit (a D/A inherits in the data driver 8, fig. 1B);

a digital video data dividing circuit for supplying picture signals to the D/A converter circuit (fig. 1B shows video data 16 bit is dividing 8 bit for each of upper data driver 8 and lower data driver 8);

a liquid crystal whose transmittivity is changed dependently on the voltage of the picture signals supplied to the pixels (see col. 5, lines 58-61);

means for supplying a first voltage for a first gradation from a D/A converter circuit to a pixel by first scanning signals of a gate driver in first subframe periods (the alternative embodiment of figs 34 and 35 show supplying a first voltage 2.1V for a grayscale level 1 is supplied in a first field VF1 of the positive frame, col. 12, lines 32-58);

means for supplying signals a voltage for a 0th gradation to the pixel by second scanning signals of the gate driver in a second subframe period (the alternative embodiment of fig. 34 shows supplying a voltage 2V for a grayscale level 0 in a second field VF2 of the positive frame, col. 12, lines 32-58);

means for supplying a second voltage for a second gradation from the D/A converter circuit to a pixel by third scanning signals of a gate driver in a third subframe period (the alternative embodiment of figs. 34 and 35 show supplying a voltage -2.2V for a grayscale level 2 in a third field of the negative frame, col. 12, lines 32-58);

means for supplying a third voltage for a third gradation from the D/A converter circuit to a pixel by fourth scanning signals of a gate driver in a fourth subframe period (the alternative embodiment of figs. 34 and 35 show supplying a voltage -2.3V for a grayscale level 3 in a fourth field of the negative frame, col. 12, lines 32-58);

means for displaying first frame by displaying a first subframe and a second subframe (the alternative embodiment of fig. 7B shows the hatching area of the display for the first field and the second field, col. 12, lines 32-58);

means for displaying second frame by displaying a third subframe and a fourth subframe (the alternative embodiment of fig. 7B shows the hatching area as shown of the display for the third field and the fourth field),

wherein first frame period has the first subframe period and the second subframe period (the positive frame has the first field and the second field, fig. 35);

wherein second frame period has the third subframe period and the fourth subframe period (the negative frame has the third field and the fourth field, fig. 35);

wherein the first subframe period and the second subframe period are adjacent to each other (the first field and the second field are adjacent, fig. 35);

wherein the third subframe period and the fourth subframe period are adjacent to each other (the third field and the fourth field are adjacent, fig. 35);

wherein the first frame is displayed gradation acknowledged by operator's eyes; the gradation is correspond to half of the first voltage (the viewer's eyes percept the hatching area is displayed the effective voltage 3 volts by taking an average of 2 volts and 4 volts, fig. 7B)

wherein the second frame is displayed combined gradation acknowledged by operator's eye (the negative frame is displayed the effective voltage 3 volts by combining with 2 volt and 4 volts, fig. 7B),

wherein the combined gradation is correspond to the second voltage and the third voltage (the combination grayscale level of the corresponding 2 volts and 4 volts, fig. 7B).

Yamaguchi fails to teach a source driver having a D/A converter circuit. AAPA conventionally discloses a digital driver including a D/A converter circuit, page 2, lines 19-26.

It would have been obvious to a person of ordinary skill at the time the invention was made to modify Yamaguchi to have the source driver having a D/A converter circuit as conventionally disclosed by AAPA. The motivation for doing so would improve the high-speed driving of the driver in the LCD device (page 2, lines 7-13 of AAPA).

Yamaguchi and AAPA fail to teach the voltage for the 0th gradation is for displaying black-display in a screen of the liquid crystal display device.

Yoshida conventionally discloses “for the remaining three frame period, the voltage between the pixel electrode 1 and the counter electrode is 0 V. Therefore, the liquid crystal cell C shuts the light and black is displayed on the screen. (Col. 2, lines 2-5; Fig. 2).

Thus, it would have been obvious to a person of ordinary skill at the time the invention was made to modify Yamaguchi and AAPA to have the voltage for the 0th gradation is for displaying black-display in a screen of the liquid crystal display device as conventionally disclosed by Yoshida. The motivation for doing so would improve the high quality of the image being displayed, while preventing flicker and ghosts (col. 3, lines 33-36 of Yoshida.)

As to claims 4 and 13, fig. 4A, col. 12, lines 59-65 of Yamaguchi shows the one frame period is 16.8ms, which implies 1/60 second.

As to claims 5 and 14, fig. 4A, col. 12, lines 59-65 of Yamaguchi shows double speed of the one frame period is 8.4ms, which implies 1/120 second.

As to claim 25, Yoshida conventionally discloses “at the second scan in one frame period, reset data (black) are written in the liquid crystal cells (col. 2, lines 56-59; fig. 2).

As to claim 26, the method of driving the liquid crystal display according to any one of claims 2 and 3, wherein the liquid crystal display device displays a low-gradation voltage area, a middle-gradation voltage area, and a high-gradation voltage area in a screen; (In the alternate embodiment, figure 25 of Yamaguchi teaches the LCD device displays darkest level at a voltage difference 0.4 volt, a middle gray scale level 8, and a brightest level at a voltage different 0 volt. (Col. 13, lines 65 to col. 14, lines 6.)

Yamaguchi fails to teach a reset signal is supplied to the one of the subframes in the low-gradation voltage area of the picture screen, and no reset signal is supplied to the one of the subframes in areas other than the low-gradation voltage area of the picture screen.

Yoshida conventionally discloses a reset data is supplied to the one of the subframes in the low-gradation voltage area of the picture screen, and write data is supplied to the one of the subframes in areas other than the low-gradation voltage area of the picture screen. (Col. 2, lines 52-67; fig. 5.)

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Yamaguchi to have the reset data is supplied to the one of the subframes in the low-gradation voltage area of the picture screen, and write data is supplied to the one of the subframes in areas other than the low-gradation voltage area of the picture screen as conventionally disclosed by Yoshida. The motivation for doing so would improve the high quality of the image being displayed, while preventing flicker and ghosts (col. 3, lines 33-36 of Yoshida.)

The limitation of claims 27 and 28 are the same as those of claim 26 and therefore the claim will be rejected using the same rationale.

7. Claims 6-9 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi in view of AAPA in view of Yoshida, and further in view of Katakura et al (US 6,057,824) hereinafter Katakura.

As to claims 6-8 and 15-17, Yamaguchi, AAPA and Yoshida teach all of the claimed limitations of claims 2, 3, 10 and 11, except for the frames are 1/24, 1/48 and 1/96 second. As modified by Katakura reference, Katakura teaches the deficiencies of Yamaguchi and AAPA in

which a related LCD device includes the frame frequency 20-40Hz and the frame scanning frequency 60-120 Hz (corresponding to the frames are 1/24, 1/48 and 1/96 second, see col. 17, lines 44-47).

As to claims 9 and 18, Katakura reviews in the related art that his invention relates to a display apparatus for use in a monitor, a video camera, a projector, a television, and a car navigation system (see col. 1, lines 10-13).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Yamaguchi, AAPA and Yoshida to become the frame frequency 20-40Hz and the frame scanning frequency 60-120 Hz (corresponding to the frames are 1/24, 1/48 and 1/96 second) as conventionally disclosed by Katakura. The motivation for doing so would provide display apparatus capable of a good halftone display while suppressing the flicker (see Katakura, col. 2, lines 3-5).

8. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi in view of AAPA in view of Yoshida, and further in view of Mikami et al (US 6,825,826) hereinafter Mikami.

As to claim 19, Yamaguchi, AAPA and Yoshida teach all of the limitation of claims 2, 3, 10 and 11, except wherein the digital video data dividing circuit and the D/A converter circuit are formed on the same substrate. As modified by Mikami reference, Mikami teaches the deficiencies of Yamaguchi and AAPA in which a related LCD comprises a D/A circuit 207 within a data driver circuit 307 including a high-speed data bus 203 and low-speed data bus 102 divided into block. These circuits are formed by the CMOSTET fabricating process on a glass substrate 305 of the display apparatus in figure 3, column 5 and 6.

As to claim 20, Mikami teaches the divided circuits 203, 102, D/A converter 207, a scan driver circuit 210, and a plurality of pixels in a pixel unit 209, which are formed on the common substrate, figure 3.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Yamaguchi, AAPA and Yoshida to form the data driver circuit 307 including a high-speed data bus 203 and low-speed data bus 102 divided into block, and the D/A circuit 207 on the common substrate 305 as taught by Mikami. The motivation for doing so would result in an advantage of being able not only to reduce power supply current of the D/A converting circuits but also to obtain a liquid crystal driving voltage that is stable and exhibits a less error even if the wiring resistance is high. The reason for the latter is that it is possible to reduce a voltage drop in the power supply wiring (see Mikami, col. 10, lines 26-31).

Response to Arguments

Applicant's arguments filed on 04/04/2008 have been fully considered but they are not persuasive. Applicant argues that Yamaguchi does not teach the feature "the liquid crystal display device displays a low-gradation voltage area, a middle-gradation voltage area, and a high-gradation voltage area in a screen." These are not found to be persuasive. In the alternate embodiment, figure 25 of Yamaguchi teaches the LCD device displays darkest level at a voltage difference 0.4 volt, a middle gray scale level 8, and a brightest level at a voltage different 0 volt. (Col. 13, lines 65 to col. 14, lines 6.

Applicant's arguments with respect to the amendment to claims 2, 3, 10, 11 and 25-28 have been considered but are moot in view of the new ground(s) of rejection.

For these reasons, the rejections have been maintained.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. NGUYEN whose telephone number is (571)272-7697. The examiner can normally be reached on MON-THU from 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571)272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KEVIN M. NGUYEN/
Primary Examiner, Art Unit 2629